Docket No.: SCEI 3.0-105

Application No.: 10/035,453

REMARKS

These remarks respond to the Office Action mailed June 27, 2005. Claims 1-4, 6, 8, 9, and 13 have been amended and claims 10, 11, and 12 were previously canceled. Therefore, claims 1-10 and 13 are pending in the application and are again presented for the Examiner's consideration in view of the following remarks. Claims 1, 6, 8, and 9 are presented in independent form.

Claim Rejections - 35 U.S.C. § 102

Claims 1-6, 8-9, and 13 were rejected under § 102 as being anticipated by Japanese Patent JP 07-141325 to Nakazawa. Referring to Fig. 1, Nakazawa discloses a signal processor with a plurality of pairs of register files (11-14) and computing elements (21-24) for parallel processing. Each pair of register files and computing elements has two input selectors (51a-54a) and (51b-54b) located between the register files and computing elements.

Amended claim 1 recites a parallel arithmetic apparatus with selecting means inserted only between one pair of recording means and operating means. Nakazawa has input selectors between every pair of register files and computing elements. Nakazawa fails to disclose or suggest selecting means inserted only between one pair of recording means and operating means. Thus, Nakazawa fails to disclose or suggest all of the elements of amended claim 1.

parallel Similarly, amended claim 6 recites arithmetic apparatus with a plurality of recording means, a plurality of operating means, and selecting means inserted only a single pair of recording means and its between Nakazawa fails to disclose or corresponding operating means. selecting means inserted between only one pair of recording means and its corresponding operating means.

Claims 8 and 9 recite an entertainment apparatus that

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performs image processing using a plurality of registers, a plurality of sum-of-products operators, and a single selector inserted between only one register and its corresponding sum-ofproducts operator. Nakazawa has two input selectors between each pair of register files and computing elements. fails to disclose or suggest an entertainment apparatus that performs image processing using only a single selector inserted between a pair of a register and a sum-of-products operator.

Claim Rejections - 35 U.S.C. § 103

Claim 7 was rejected under § 103 as obvious over Claim 7 is asserted as patentable at least for the reasons discussed above in connection with claim 6, upon which claim 7 depends.

Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate If, however, for any reason the condition for allowance. Examiner does not believe that such action can be taken at this is respectfully requested that he/she telephone it applicant's attorney at (908) 654-6325 in order to overcome any additional objections which he/she may have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: September 20, 2005 Respectfully submitted,

Matthew E. Hanley

Registration No.: 51,773 LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK, LLP 600 South Avenue West Westfield, New Jersey 07090 (908) 654-5000

Attorney for Applicant

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